

R2 UMA(11.6")

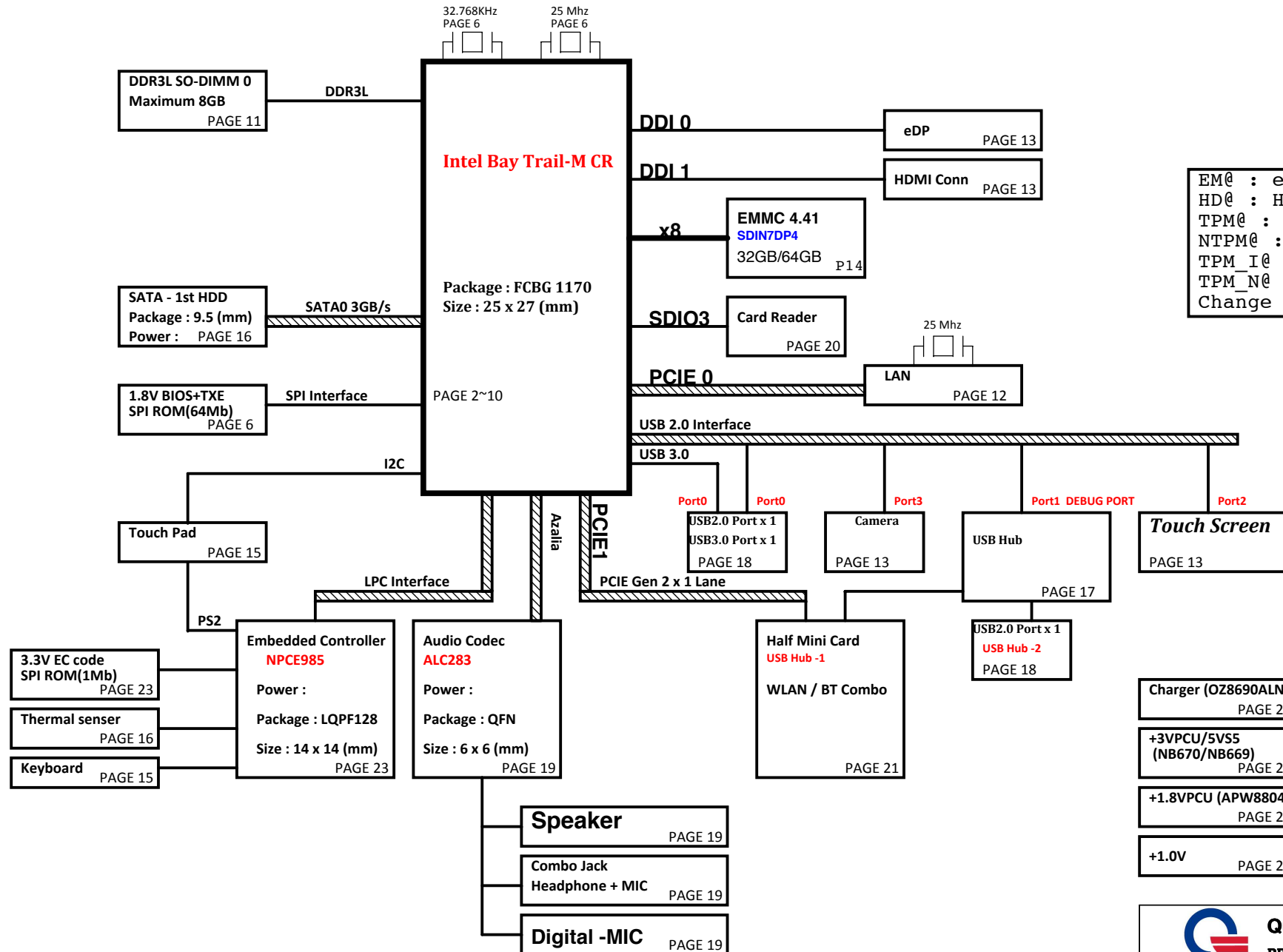
01

Intel Bay Trail-M Platform Block Diagram

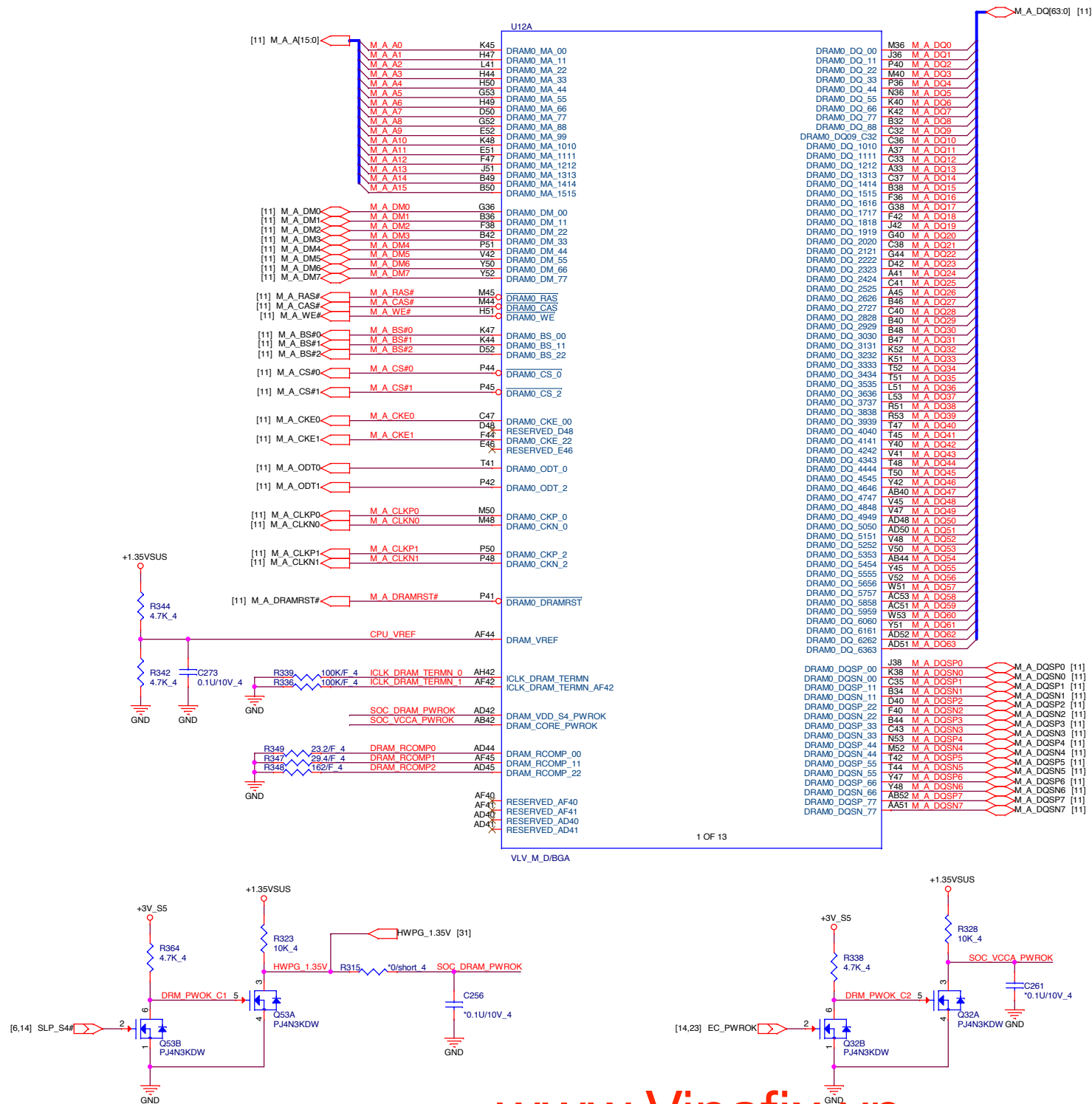
PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

EM@ : eMMC
HD@ : HDD
TPM@ : TPM
NTPM@ : Non-TPM
TPM_I@ : 新唐
TPM_N@ : 英飛凌
Change CPU & EMMC P/N



Charger (OZ8690ALN) PAGE 25	+1.05V/1.5V PAGE 29
+3VPCU/5V55 (NB670/NB669) PAGE 26	+VCORE+VGFX(ISL95833) PAGE 30
+1.8VPCU (APW8804) PAGE 27	DDR3 (APW8819) PAGE 31
+1.0V PAGE 28	Dis-charge IC (G5934) PAGE 32



U12B

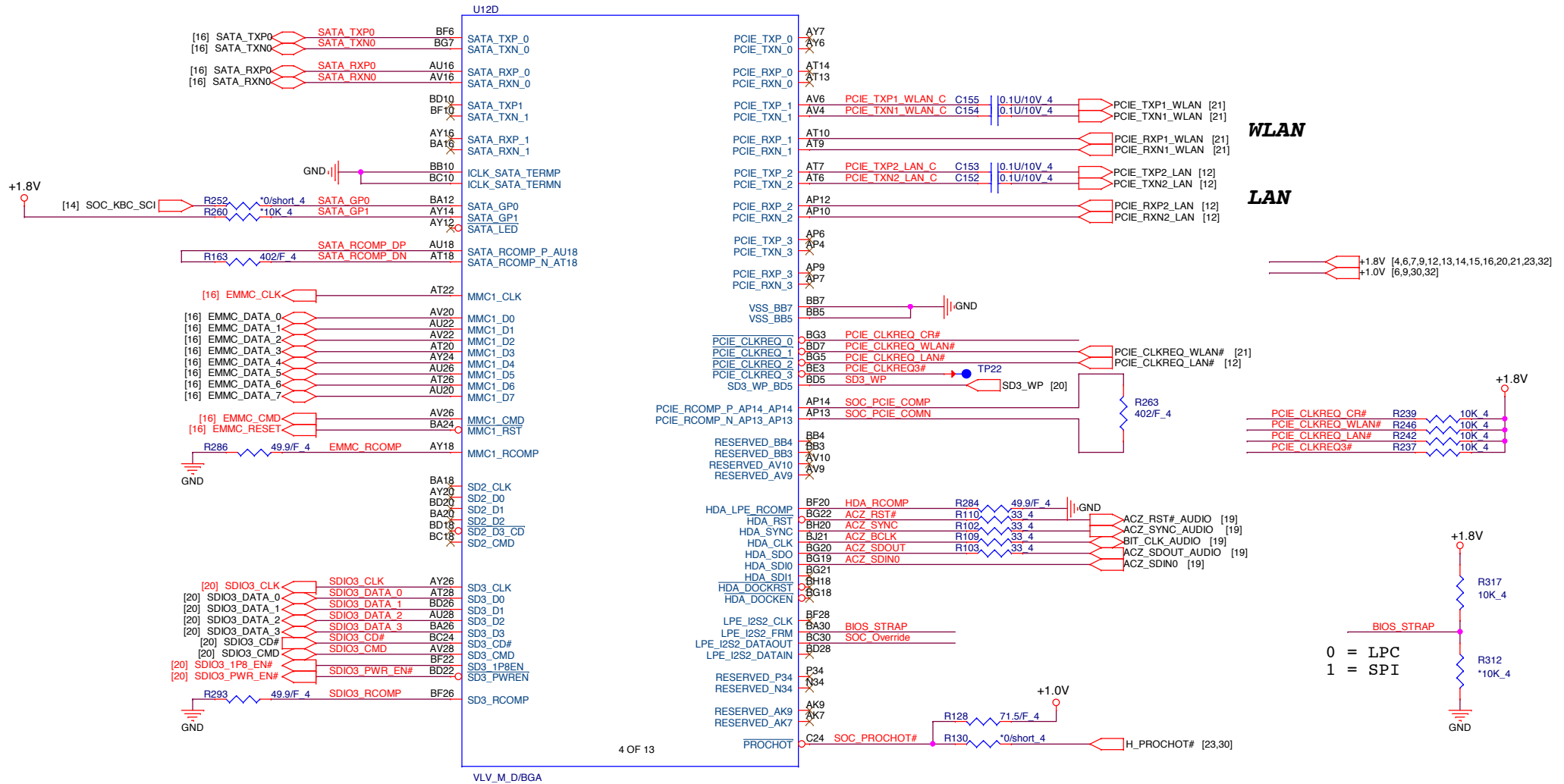
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BB47
AW41
BB44
BB50
BC53
BB49
BF50
BC52
BE52
AY48
BE51
BD47
BA51
BH49
BH50
BD38
BH36
BC36
BH42
AT51
AM42
AK50
AK52
AV45
AV44
BB50
AY47
AY44
BF52
AT44
AT45
BG47
BE46
BD44
BF48
AP41
AT42
AV50
AV48
AT50
AT48
AT41

DRAM1_MA_00
DRAM1_MA_11
DRAM1_MA_22
DRAM1_MA_33
DRAM1_MA_44
DRAM1_MA_55
DRAM1_MA_66
DRAM1_MA_77
DRAM1_MA_88
DRAM1_MA_99
DRAM1_MA_1010
DRAM1_MA_1111
DRAM1_MA_1212
DRAM1_MA_1313
DRAM1_MA_1414
DRAM1_MA_1515
DRAM1_DM_00
DRAM1_DM_11
DRAM1_DM_22
DRAM1_DM_33
DRAM1_DM_44
DRAM1_DM_55
DRAM1_DM_66
DRAM1_DM_77
DRAM1_RAS
DRAM1_CAS
DRAM1_WE
DRAM1_BS_00
DRAM1_BS_11
DRAM1_BS_22
DRAM1_CS_0
DRAM1_CS_2
DRAM1_CKE_00
RESERVED_BE46
DRAM1_CKE_22
RESERVED_BF48
DRAM1_ODT_0
DRAM1_ODT_2
DRAM1_CKP_0
DRAM1_CKN_0
DRAM1_CKP_2
DRAM1_CKN_2
DRAM1_DRAMRST

DRAM1_DQ_00
DRAM1_DQ_11
DRAM1_DQ_22
DRAM1_DQ_33
DRAM1_DQ_44
DRAM1_DQ_55
DRAM1_DQ_66
DRAM1_DQ_77
DRAM1_DQ_88
DRAM1_DQ_99
DRAM1_DQ_1010
DRAM1_DQ_1111
DRAM1_DQ_1212
DRAM1_DQ_1313
DRAM1_DQ_1414
DRAM1_DQ_1515
DRAM1_DQ_1616
DRAM1_DQ_1717
DRAM1_DQ_1818
DRAM1_DQ_1919
DRAM1_DQ_2020
DRAM1_DQ_2121
DRAM1_DQ_2222
DRAM1_DQ_2323
DRAM1_DQ_2424
DRAM1_DQ_2525
DRAM1_DQ_2626
DRAM1_DQ_2727
DRAM1_DQ_2828
DRAM1_DQ_2929
DRAM1_DQ_3030
DRAM1_DQ_3131
DRAM1_DQ_3232
DRAM1_DQ_3333
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DRAM1_DQ_4141
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DRAM1_DQ_4646
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DRAM1_DQ_5555
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DRAM1_DQ_5757
DRAM1_DQ_5858
DRAM1_DQ_5959
DRAM1_DQ_6060
DRAM1_DQ_6161
DRAM1_DQ_6262
DRAM1_DQ_6363
DRAM1_DQSP_00
DRAM1_DQSN_00
DRAM1_DQSP_11
DRAM1_DQSN_11
DRAM1_DQSP_22
DRAM1_DQSN_22
DRAM1_DQSP_33
DRAM1_DQSN_33
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DRAM1_DQSN_44
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DRAM1_DQSN_77

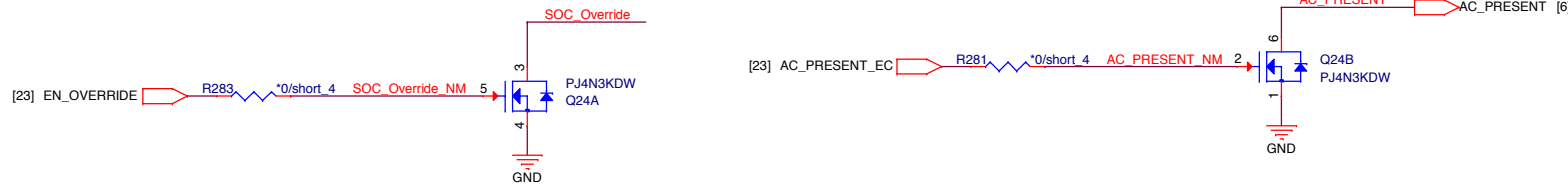
BG38
BC40
BA42
BD42
BC38
BD36
BF42
BC44
BH32
BG32
BG36
BJ37
BG33
BJ33
BG37
BH38
AU36
AT36
AV40
AT40
BA36
AV36
AY42
AY40
BJ41
BG41
BJ45
BH46
BG40
BH40
BH48
BH47
AY52
AY51
AP52
AP51
AW51
AW53
AR51
AR53
AP47
AP45
AK40
AM41
AP48
AP50
AK42
AH40
AM45
AM47
AF48
AF50
AM48
AM50
AH44
AK45
AM52
AL51
AG53
AG51
AL53
AK51
AF52
AF51
BF40
BD40
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BA38
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AK48
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AJ51

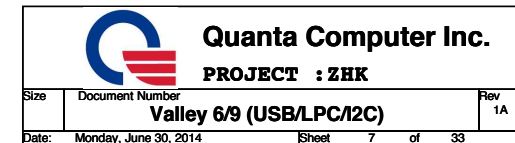


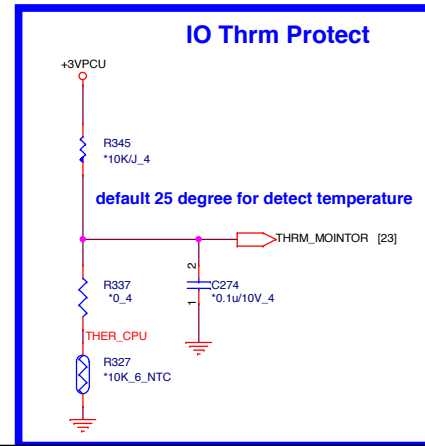
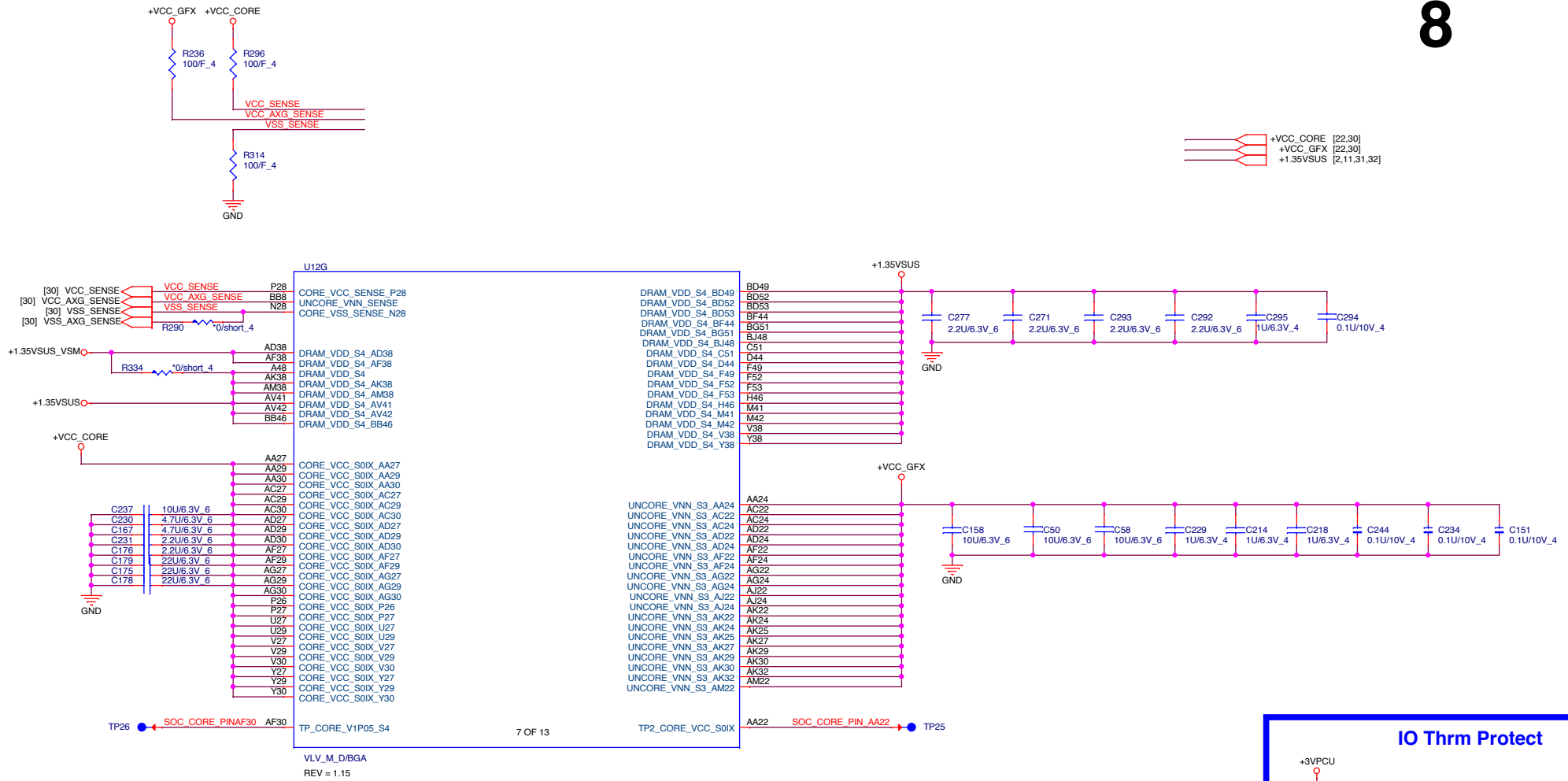


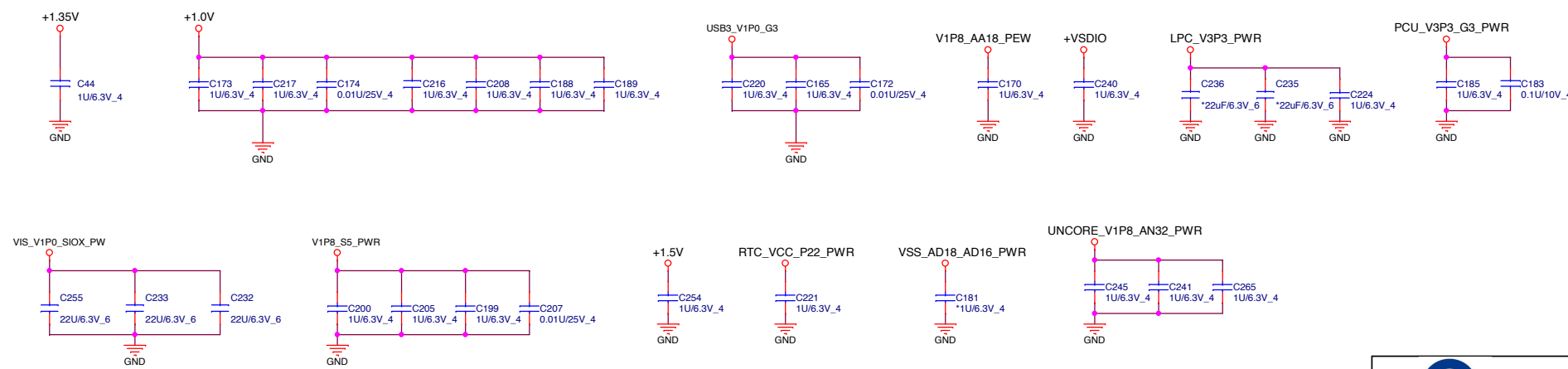
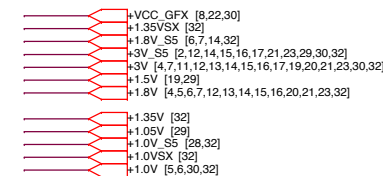
Security Flash Descriptors
0 = Override
1 = Normal Operation

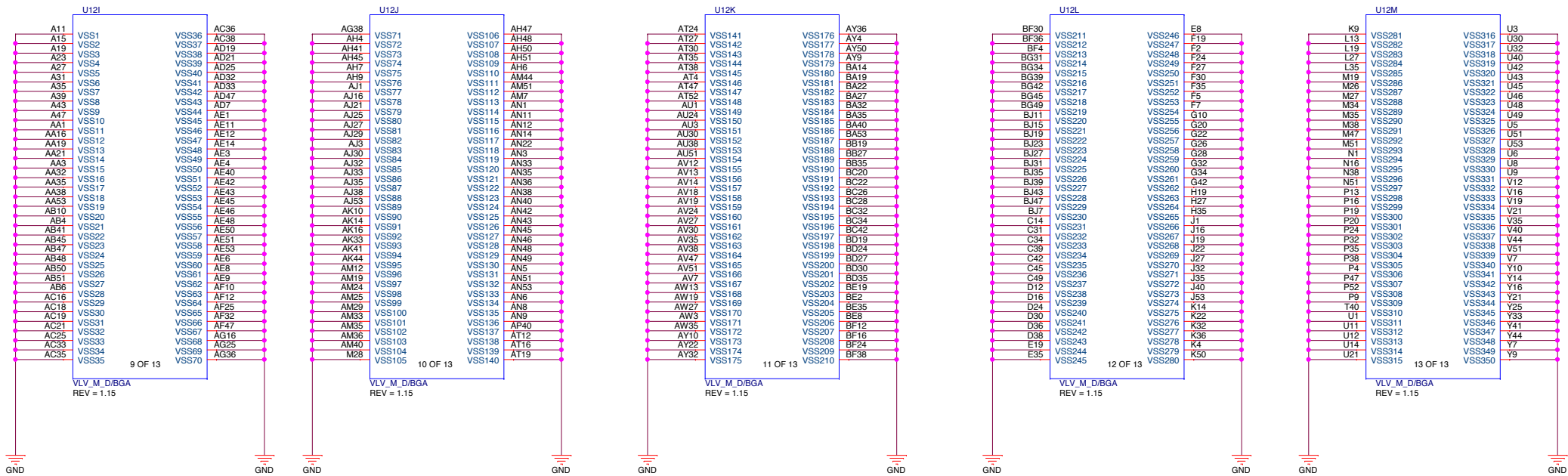
AC Present: This input pin indicates when the platform is plugged into AC power.

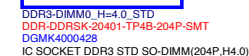






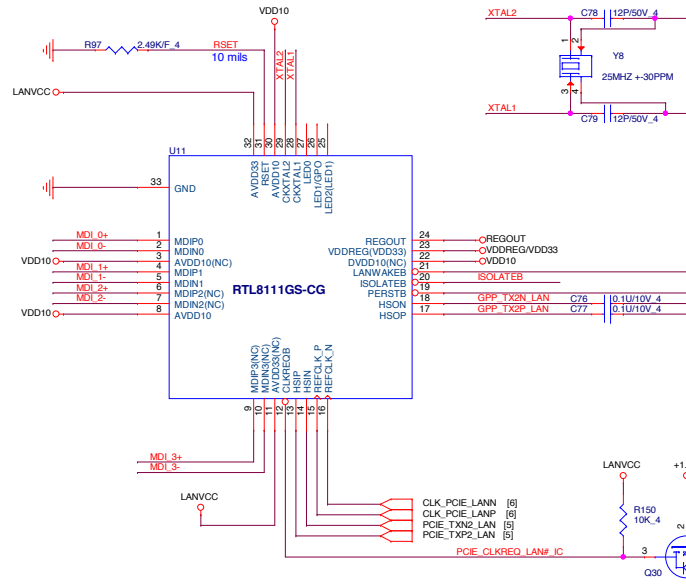
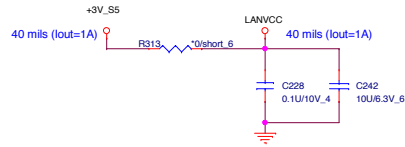






LANVCC

[2,9,14,15,16,17,21,22,29,30,32]
[4,7,8,11,13,14,15,16,17,19,20,21,23,30,32]



For RTL8111G(S)
* Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30

For RTL8111GS
* Place 0.1uF CAP close to each VDD33 pin-- 11, 32

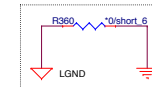
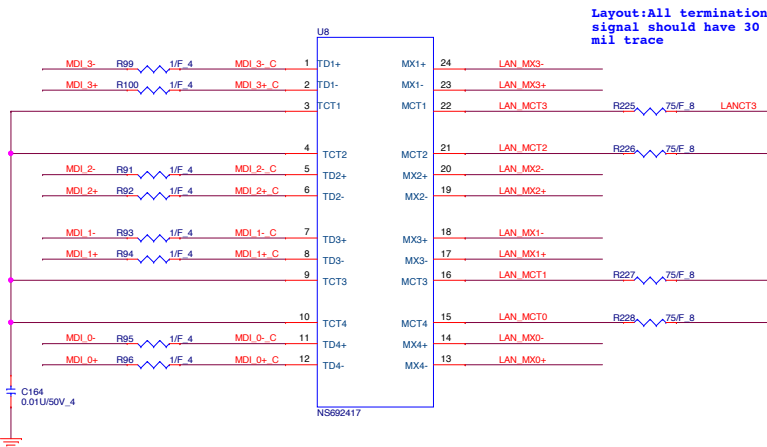
Close to pin 11,32

Remove For Not Using SWR mode
~~C403, C404~~ ~~Pin23~~.

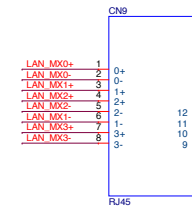
Rev: B (C-test) L13 Remove CV-4708MN00 for SMT request, change P/N to CV-4710T201

For RTL8111G(S)
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)

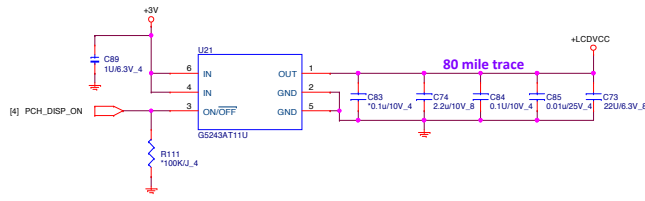
Transformer



RJ45 Connector

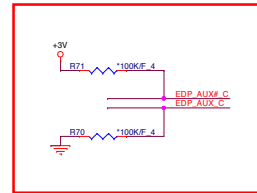
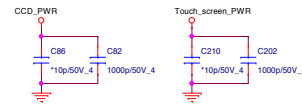
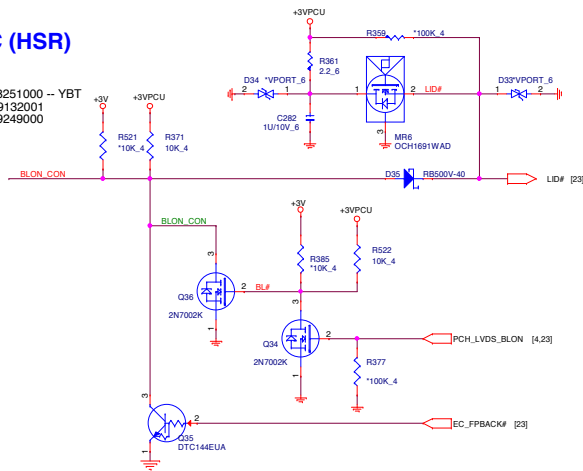


Rev: B (C-test) CN9 change main source P/N to DFTJ08FR414
2nd source : DFTJ08FR417

LVDS Conn.

HALL IC (HSR)

1st source : EOD
2nd source : AL008251000 --
3rd source : AL009132001
4th source : AL009249000

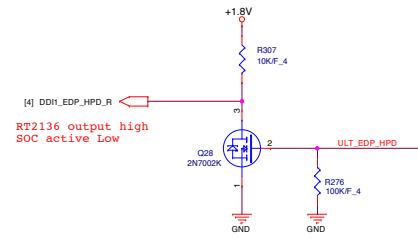
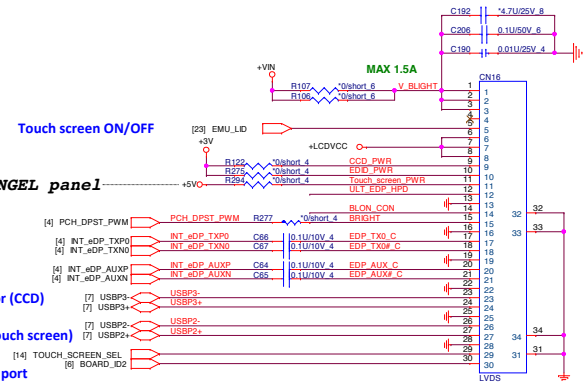


For ANGEL panel

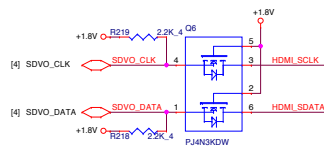
USB to Connector (CCD)

USB to Connector (Touch screen)

Touch screen SEL. [14]
Auto enable/disable touch panel USB port

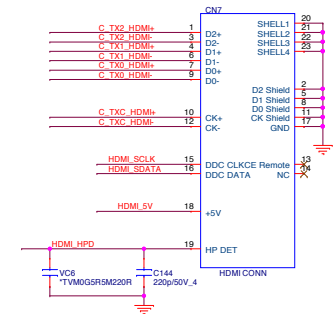
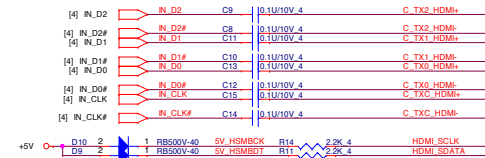
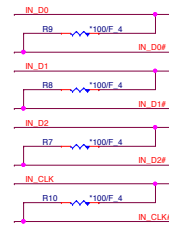


[4,7,9,11,12,14,15,16,17,19,20,21,23,30,32]	+3V
[4,5,6,7,9,12,14,15,16,20,21,23,32]	+1.8V
[16,19,32]	+5V

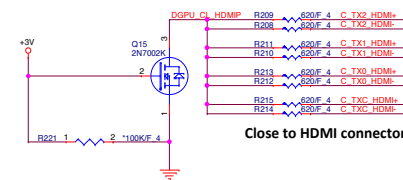
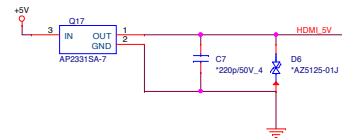
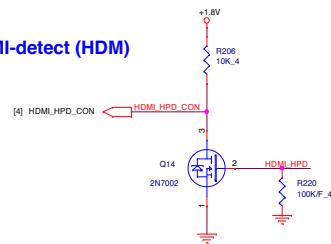
**HDMI Conn.**

HDMI SMBus Isolation

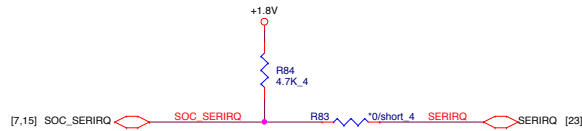
EMI (EMC)



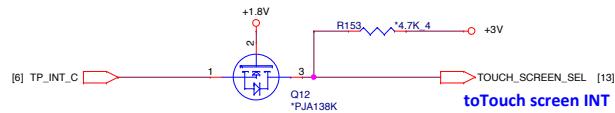
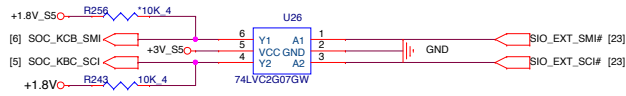
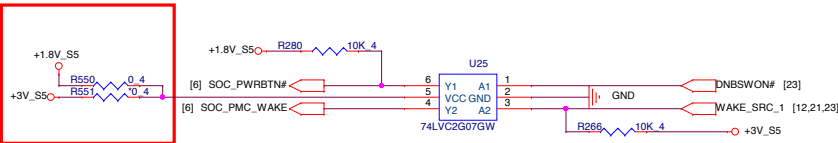
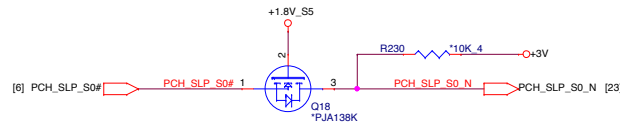
HDMI-detect (HDM)



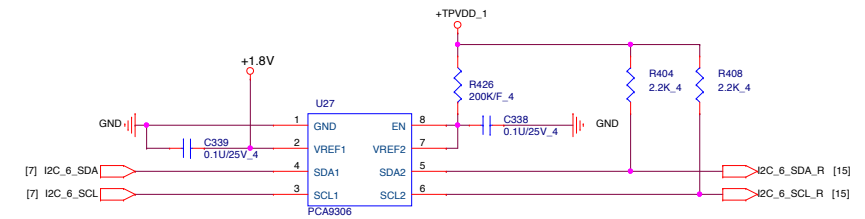
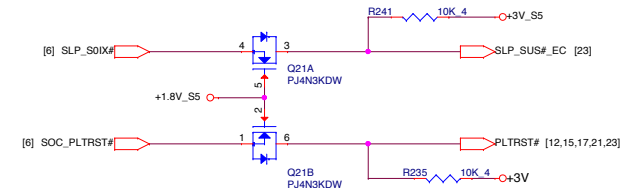
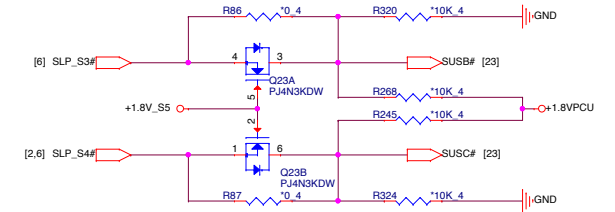
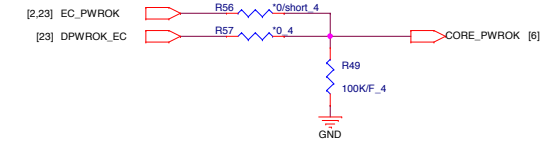
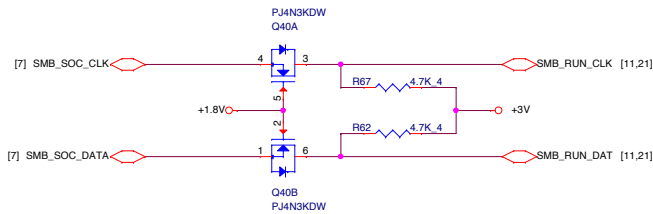
[6,7,9,32] +1.8V_S5
[2,9,12,15,16,17,21,23,29,30,32] +3V_S5
[4,5,6,7,9,12,13,15,16,20,21,23,32] +1.8V
[4,7,9,11,12,13,15,16,17,19,20,21,23,30,32] +3V



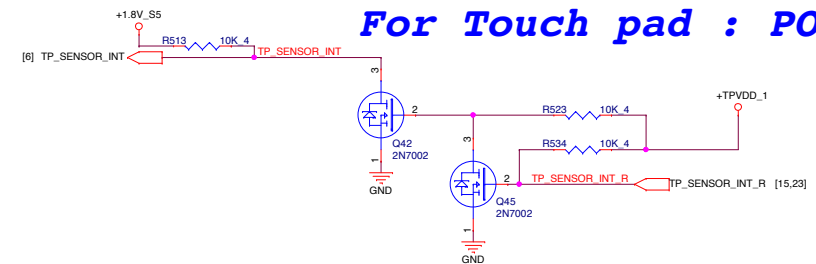
Reserve for +1.8V new EC




toTouch screen INT



For Touch pad : POWER-A



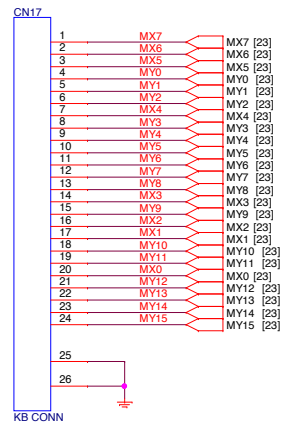


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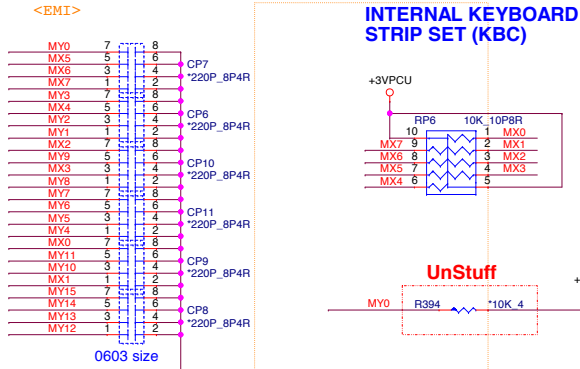
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	Level Shifter	1A
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KEYBOARD (KBC)

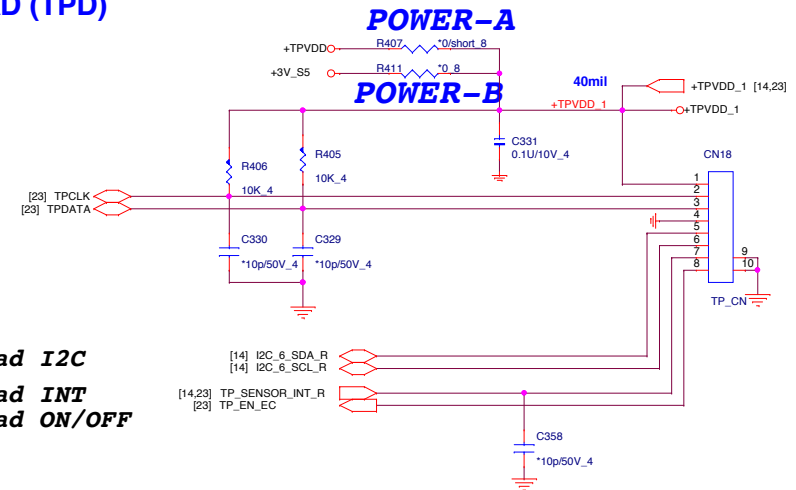
<20110214(E1A)>
Change CP1~CP6 footprint from
8p4r-0402-smt to 8P4R, for SMT open issue.



Rev: B (C-test) CN17 change ACS P/N from DFFC24FR000 to DFFC24FR110



TOUCH PAD (TPD)

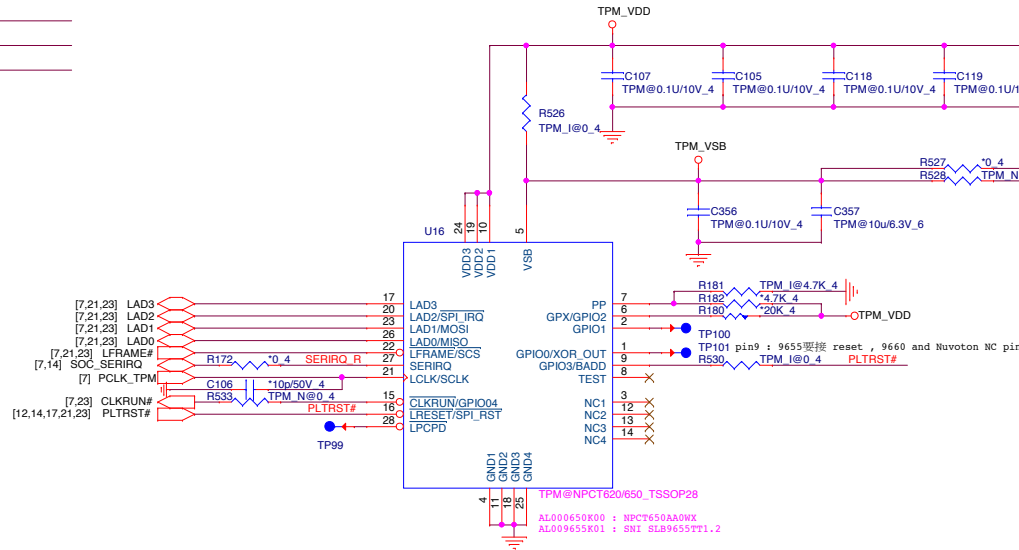
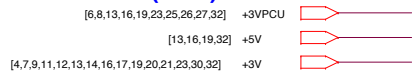


Touch pad I2C
Touch pad INT
Touch pad ON/OFF

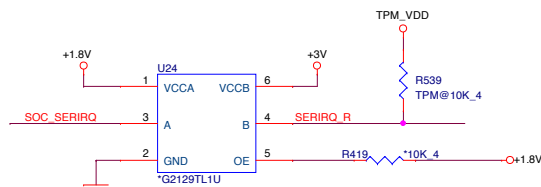
15

```
ACER DEFINE
VDD
PS2-CLK
PS2-DATA
GND
I2C-DATA
I2C-CLK
ATTN (INT)
SER-OFF.
```

TPM (TPM)



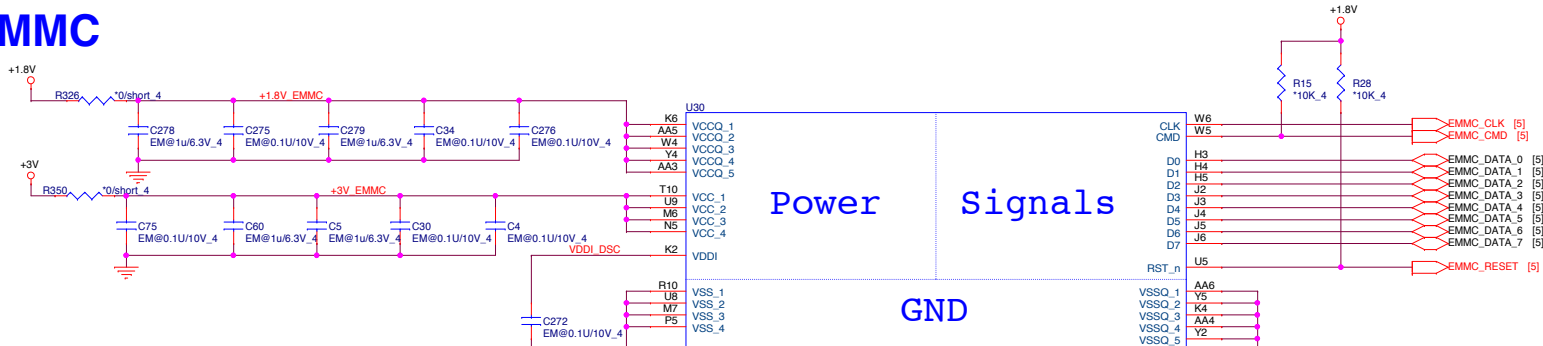
```
TPM_N for 新唐
TPM_I for 英飛凌---- default
```



note: serie need to add level shift

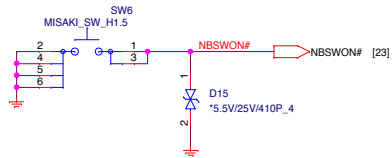
eMMC

16

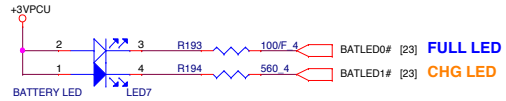


+5V [13,19,32]
+3VPCU [6,8,13,15,19,23,25,26,27,32]
+3V [4,7,9,11,12,13,14,15,17,19,20,21,23,30,32]
+3V_SS [2,9,12,14,15,17,21,23,29,30,32]

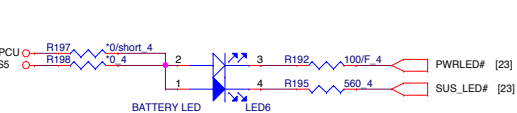
PWR button



Battery indicator

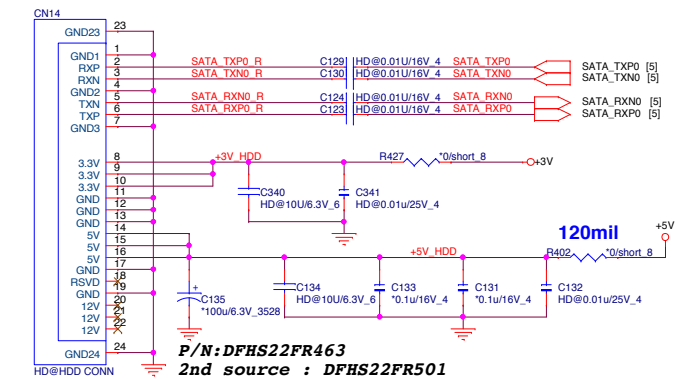


PWR indicator

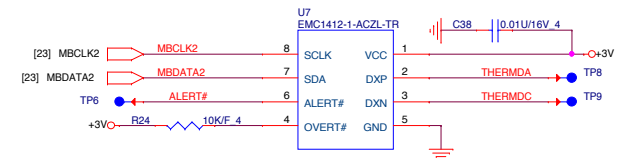


NC

SATA HDD



CPU Thermal sensor(THS) / MB Local TEMP



Main:AL001412003
2nd:AL000431014

EMC1412-1-ACZL-TR(98h)
TMP431ADGKR(98h)



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Size	Document Number	Rev
	HDD/HalVeMMC/LED	1A
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[6,26,28,29,30,31,32] +5V_S5

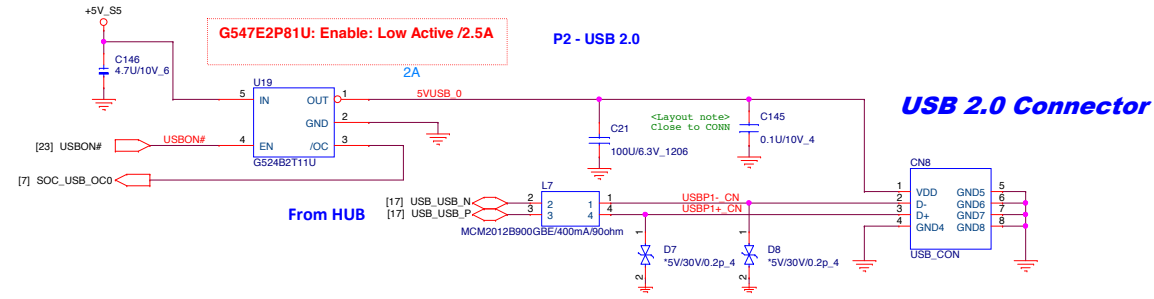
From APU

From APU

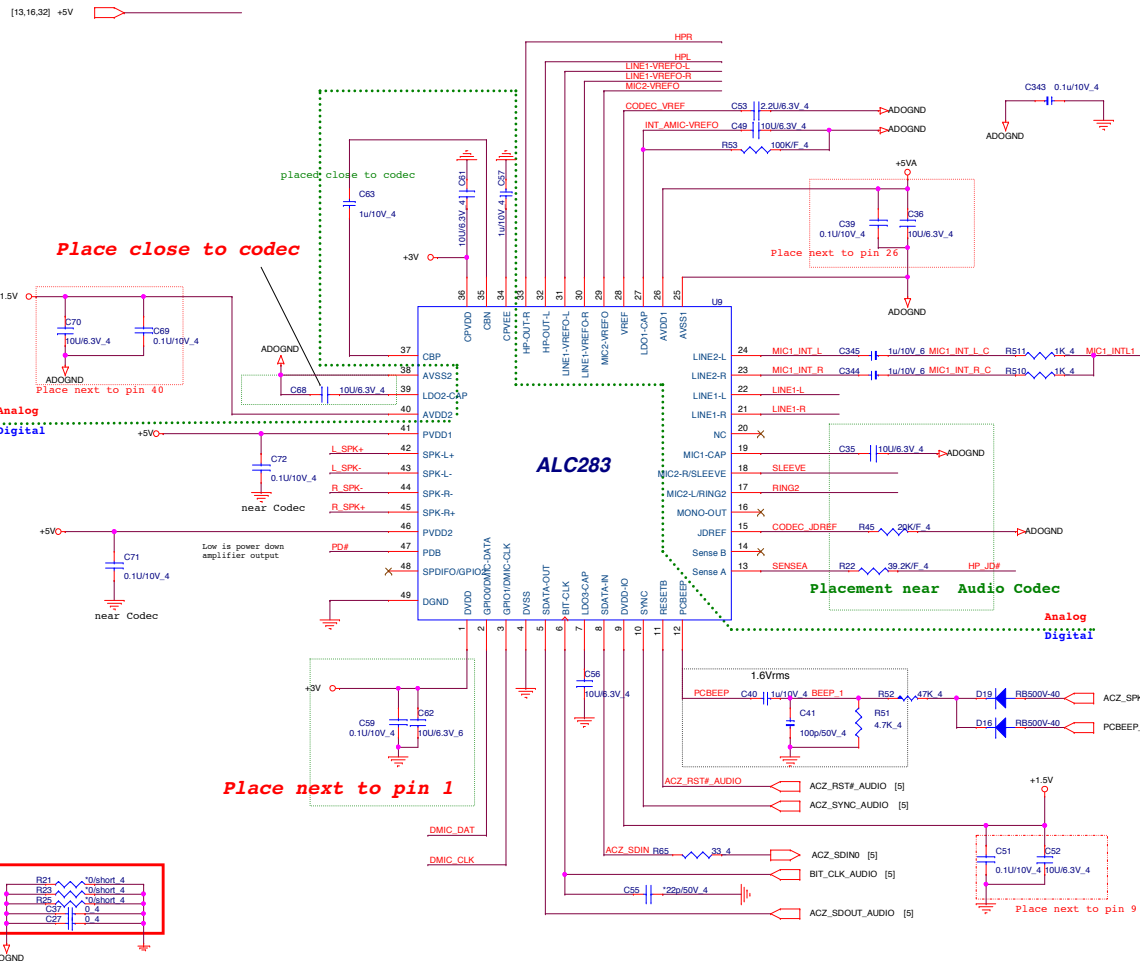
Close USB3.0

USB2.0 connector P/N:
DFHS04FR487

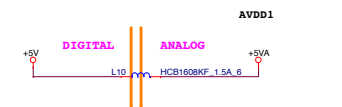
USB 3.0 Connector



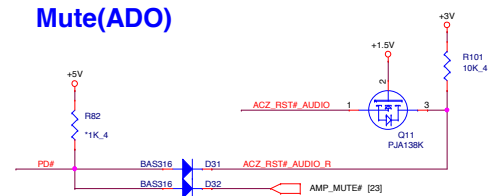
Codec(ADO)



Codec PWR 5V(ADO)

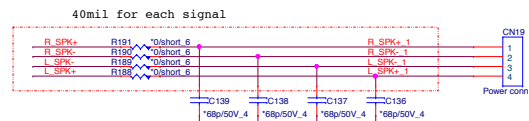


Mute(ADO)



Internal Speaker

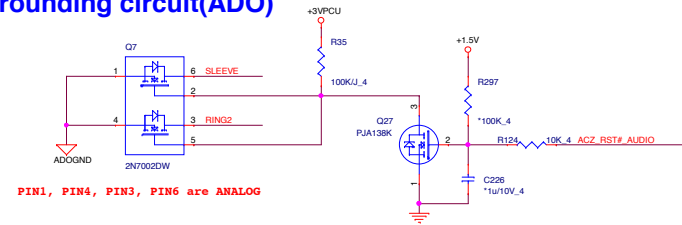
footprint 88266-040xx-xxx-4p-1



20130515 swap pin by ME.

Rev: B (C-test) CN19 change ACS P/N from DFHD04MRA75 to DFHD04MR211

Grounding circuit(ADO)



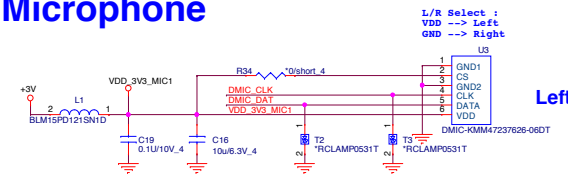
PIN1, PIN4, PIN3, PIN6 are ANALOG

INT MIC array

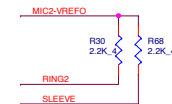


cap place close to MIC-connector

Microphone

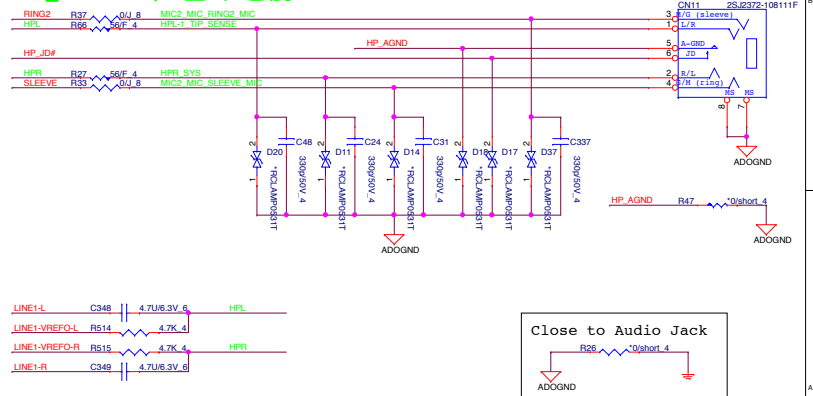


Left



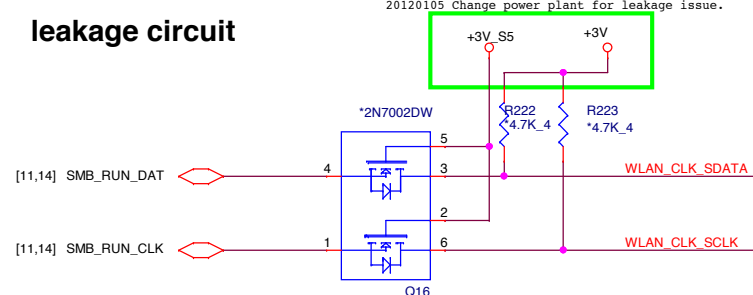
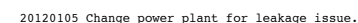
note : change next P/N: DFTJ06FR653
CONN DIP PHONE JACK 6P FR(H4.5)
foot print: phjk-2sj3072-108111f-6p


HP_MIC 上/下/左/右包覆AGND

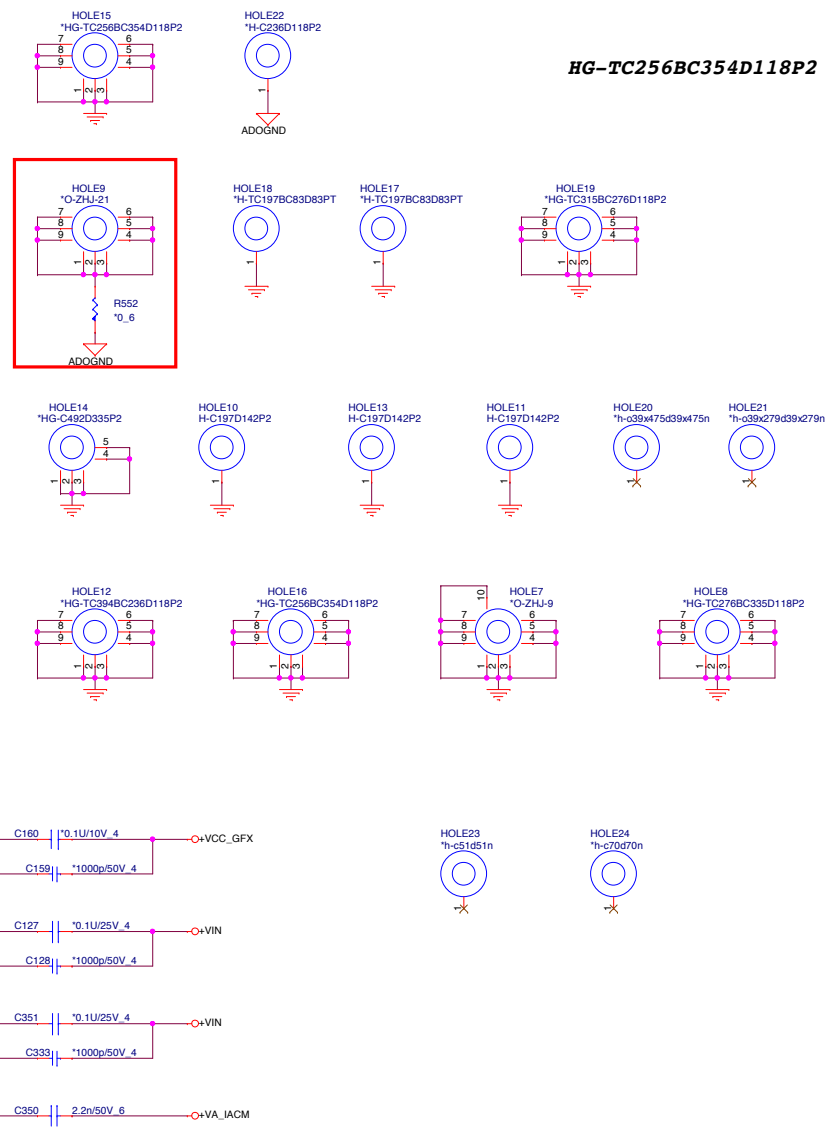


Close to Audio Jack





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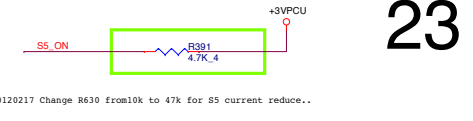


note: PR173 change to 1.5k/F
CS21502FB14 RES CHIP 1.5K +-1% 1/16W(0402)

For EC control thermal protection (output 3.3V)

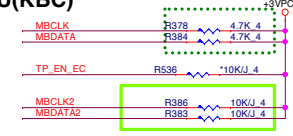
1.8V p/n: AJ009850F02
Discription: IC CONTROLLER (128P) NPCE985LB1DX (LQFP)

Note:
GPIO75 EMU_LIDTouch panel enable/disable#Follow ZEA --->ZHJ None
GPIO70 TP_EN_EC Touch pad enable/disable# --->ok
GPIO27 TP_INT_EC#Touch pad interrupt

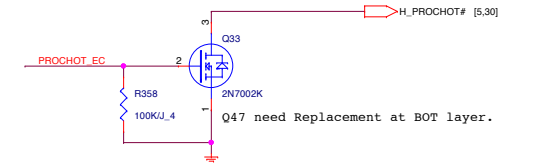


20120217 Change R630 from 10k to 47k for S5 current reduce..

SM BUS PU(KBC)

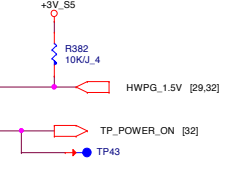


2013/07/31
SMbus Tr fail (spec 1000 ns max, result 1046 ns)
Change PU resistor (R424, R428) from 10K to 4.7K

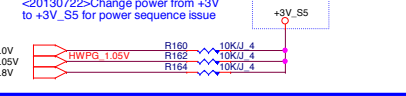


Q47 need Replacement at BOT layer.

HWPG(KBC)



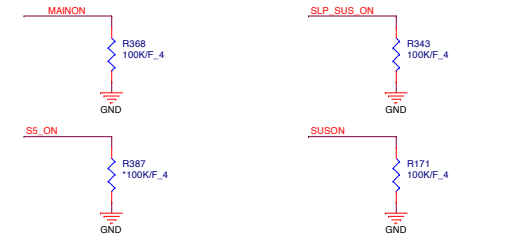
Note: GPIO75 (pin82) for TOUCHPANEL_ON
pin91 in 985L is 1.8V only



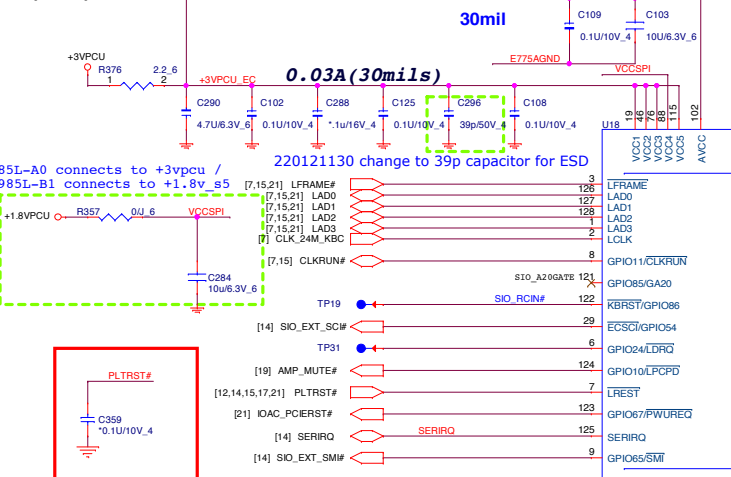
<20130722>Change power from +3V to +3V_S5 for power sequence issue

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU



EC(KBC)



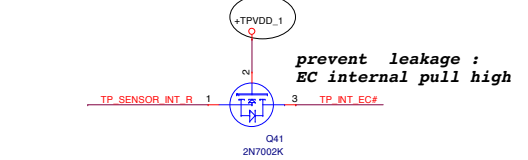
Reserve R477, R478 for EC chip PU function issue.

pin14 +VCC_GFX
pin22 +3V_D for ATI
pin24 +1V for ATI
pin26 +1.8V_GPU for ATI
pin28 GPU_RESET

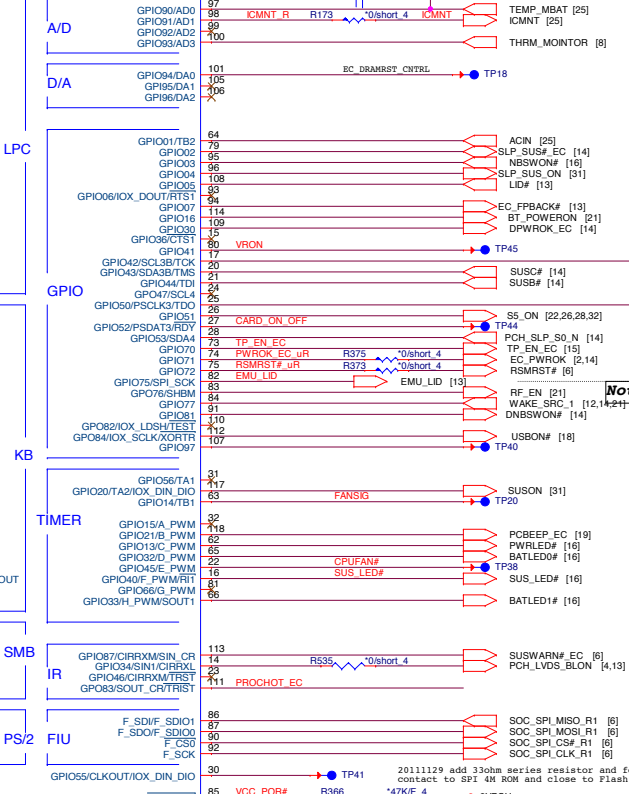
note: gpio27 -->TOUCH_PAD_INT

Reserve for writing ME ROM

PCI interface should be used on Bay Trail platform, thus VTT pin can wire to GND and PRC1 signal can be left un-connected.




prevent leakage :
EC internal pull high

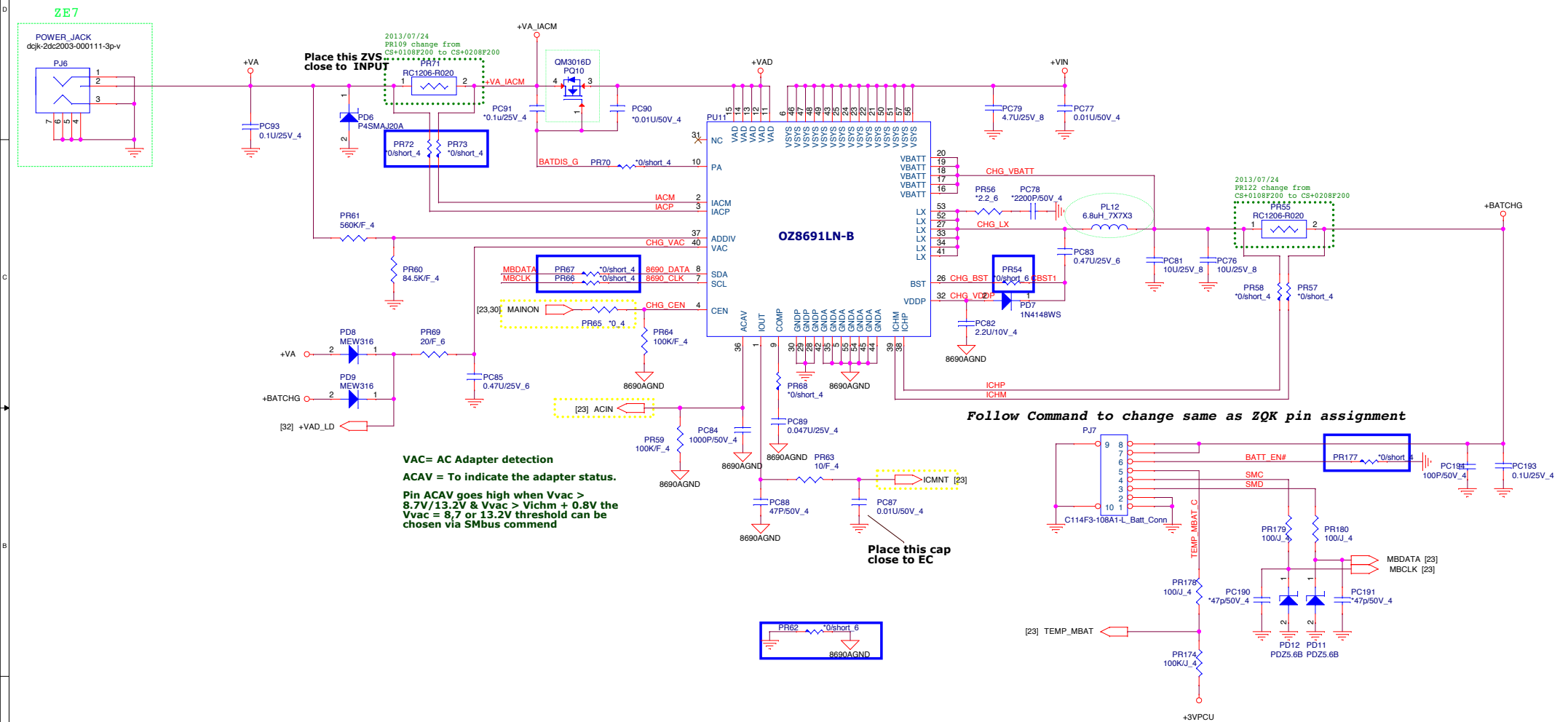


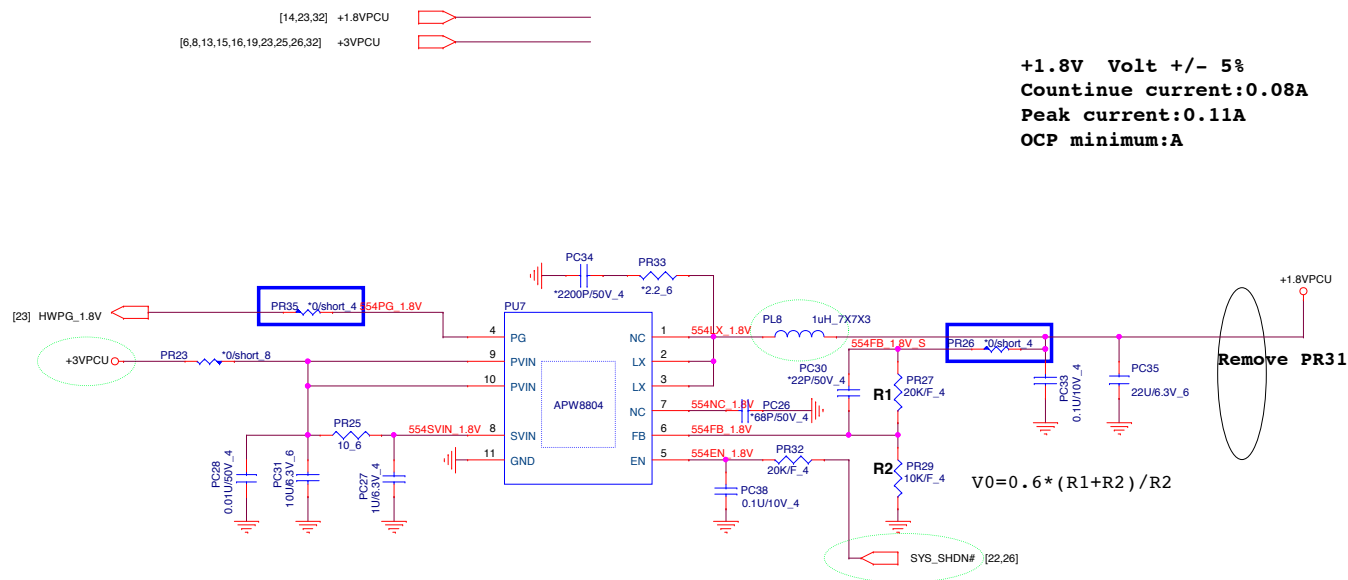
Bay Trail-M S4/S5 to S0 (Power Up) Sequence

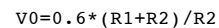
24



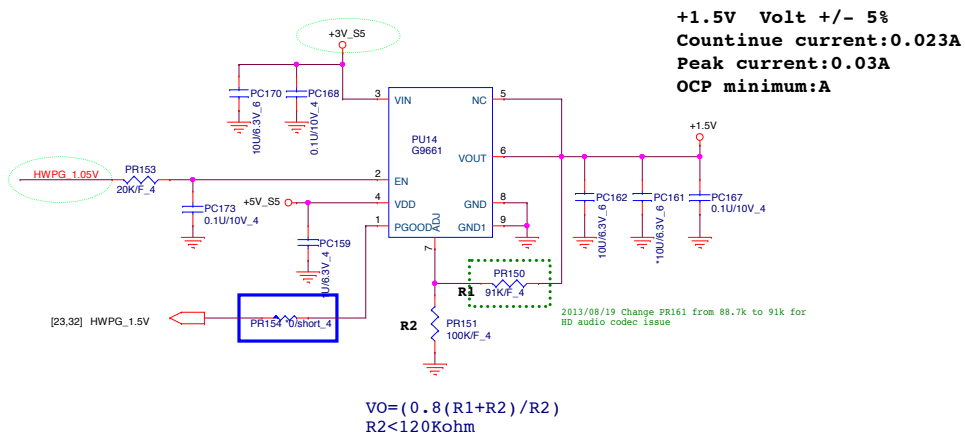
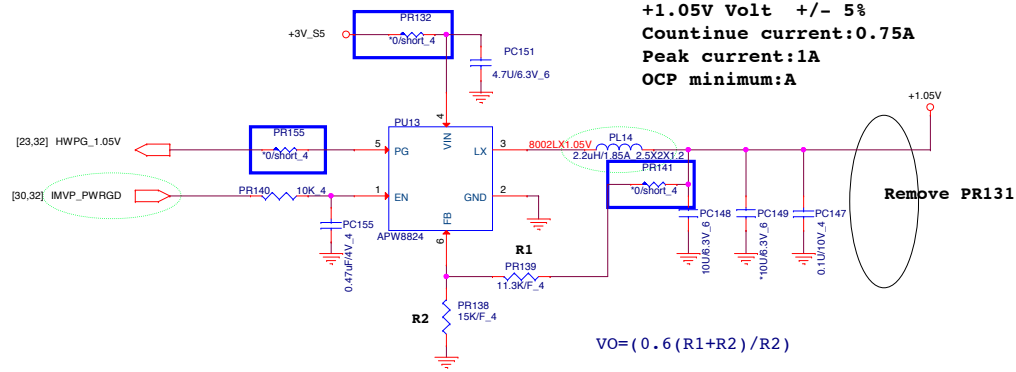
		Quanta Computer Inc.	
		PROJECT : ZHK	
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	Power sequence		1A
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[2,9,12,14,15,16,17,21,23,30,32] +3V_S5
 [9] +1.05V
 [9,19] +1.5V



20130617 Change +1.05V to +1.0V

